

**GATE LINEWIDTH TAILORING AND CRITICAL DIMENSION
CONTROL FOR SUB-100 NM DEVICES USING PLASMA ETCHING**

ABSTRACT

5 A method of fabricating an electronic chip on a wafer in which a first mask
at a predetermined lower resolution is developed on the wafer and then etched
under a first set of conditions for a predetermined period to achieve a mask that is
below the resolution limit of current lithography. The etched mask is then used as
a hard mask for etching material on a lower layer.

FIS920010077US1